TK

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,044	09/29/2003	David M. Callaghan	03AB015/ALBRP324US	2584

7590 05/15/2006

Susan M. Donahue
Rockwell Automation, 704-P
IP Department
1201 South 2nd Street
Milwaukee, WI 53204

EXAMINER	
URICK, MATTHEW T	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/674,044	CALLAGHAN, DAVID M.	
	Examiner	Art Unit	
	Matt Urick	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 September 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 29 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Claims

Claims 1-10, 13-15, 17, 20-23, 25-29, 34, 35, and 42 are rejected under 35 USC 102

Claims 11, 12, 16, 18, 19, 24, 30-33, and 36-41 are rejected under 35 USC 103

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (United States Patent No. 6,141,768).

As per claim 1, Lin discloses:

A self-testing random access memory system, comprising:

a memory array (column 4 lines 33-38); and

a self-testing RAM interface embedded on a circuit board with the memory array, the self-testing RAM interface tests integrity of data stored in the memory array (column 4 lines 33-38).

As per claim 2, Lin discloses:

The system of claim 1, the self-testing RAM interface interacts with a central processing unit (CPU) to test the CPU to memory interface (column 4 lines 6-10).

As per claim 3, Lin discloses:

The system of claim 1, the self-testing R.AM interface cooperates with a CPU to facilitate testing memory array data cells (column 4 lines 6-10).

As per claim 4, Lin discloses:

The system of claim 1, the self-testing RAM interface can correct errors in data stored in the memory array (column 4 lines 54-61).

As per claim 5, Lin discloses:

The system of claim 4, the self-testing RAM interface corrects errors by replacing erroneous data with redundant data stored in the memory array (column 5 lines 22-32).

As per claim 6, Lin discloses:

The system of claim 1, the self-testing RAM interface includes a microprocessor (column 6 lines 30-31).

As per claim 7, Lin discloses:

The system of claim 6, the self-testing R.AM interface includes a memory component that facilitates execution of testing and/or correcting algorithms (column 4 lines 33-36).

As per claim 8, Lin discloses:

The system of claim 1, the self-testing interface is implemented with discrete logic (column 4 lines 36-38).

As per claim 9, Lin discloses:

The system of claim 1, the self-testing RAM interface is implemented using SOC (System on Chip) technology (column 10 lines 19-22).

As per claim 10, Lin discloses:

The system of claim 1, the memory array is associated with a field programmable gate array (column 4 lines 16-18).

As per claim 13, Lin discloses:

The system of claim 1, the self-testing RAM interface supports multi-port memory Access (column 4 lines 1-23).

Claims 14, 15, 17, 34, 35, and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig (US Patent No. 6,505,305).

As per claim 14, Olarig discloses:

A self-testing and self-validating memory system comprising:

one or more memory storage banks (column 10 lines 59-65); and

at least one central processing unit (CPU) with a self-testing RAM interface subsystem for ensuring correct data retrieval (column 10 lines 59-65).

As per claim 15, Olarig discloses:

The system of claim 14, the storage banks comprising standard RAM components with internal flaws (column 13 lines 55-59)

As per claim 17, Olarig discloses:

The system of claim 14, the self-testing RAM interface comprises large geometry devices (column 5 lines 38-45: memory module is large geometry) and ECC (column 5 lines 17-20), wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory storage banks .

As per claim 34, Olarig discloses:

A method of reading data from a self-testing RAM device comprising:

choosing a memory address (column 10 lines 59-65);

retrieving data from a memory location associated with the address (column 10 lines 59-65);

determining whether the data is correct (column 10 lines 59-65);

correcting the data if it is incorrect (column 11 lines 3-20); and

outputting the data to the requesting device, wherein the method disclosed hereby is performed by a self-testing RAM interface (column 12 lines 44-48).

As per claim 35, Olarig discloses:

The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by utilizing an error correction code (column 5 lines 11-20).

As per claim 42, Olarig discloses:

An article of manufacturing comprising a computer usable medium having computer readable program code means thereon to perform the method of claim 34 (column 7 lines 43-46)

Claims 14, 17, 34, 35, and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Callaway (United States Patent No. 6,879,530).

As per claim 20, Callaway discloses:

A self-correcting and self-validating device comprising:

a plurality of internal memory stores; and a self-testing interface that maps input addresses and data to a multitude of memory cells on a plurality of memory stores to facilitate accurate data storage and retrieval, wherein the memory cells store copies of the input data (column 10 lines 30-51).

Claims 22, 23, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayes (US Patent 5,781,721).

As per claim 22, Hayes discloses:

A method of self-testing comprising:

writing values to one or more memory cells in a memory device (column 4 lines 56-61),

reading the values stored by the one or more memory cells (column 4 lines 62-67);

comparing the values written with the values read (column 4 lines 62-67); and

notifying a central processing unit if any of the values written differ from the values read, wherein writing values, reading a value, comparing values, and notifying a central processing unit are performed by a self-testing RAM interface (column 5 lines 31-37).

As per claim 23, Hayes discloses:

The method of claim 22, the values written correspond to a test pattern (column 4 lines 62-67).

As per claim 25, Hayes discloses:

The method of claim 22, the self-testing RAM interface is embedded on the same device as the memory cells (column 5 lines 14-21).

As per claim 26, Hayes discloses:

The method of claim 22, further comprising bringing the memory device on-line for use upon successful test completion (column 5 lines 10-13).

As per claim 27, Hayes discloses:

An article of manufacturing comprising a computer usable medium having computer readable stored instructions thereon to perform the method of claim 26 (column 5 lines 14-17).

Claims 22, 23, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayes (US Patent 5,781,721).

As per claim 28, Crouch discloses:

A method for testing a central processing unit (CPU) to memory interface comprising: loading a data pattern into CPU registers (column 5 lines 14-26);

writing the pattern from the registers to at least a portion of memory in a memory device (column 5 lines 14-26)

reading the data written to each memory cell (column 15 lines 15-35);

comparing the data written with the data expected in accordance with the pattern (column 15 lines 15-35);

notifying the CPU if any data read is different than the data expected, wherein reading the data, comparing the data, and notifying the CPU are performed by a self-testing RAM interface (column 15 lines 15-35).

As per claim 29, Crouch discloses:

An article of manufacturing comprising a computer usable medium having computer readable instructions stored thereon to perform the method of claim 28 (column 15 lines 15-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (United States Patent No. 6,141,768) in view of Microsoft Computer Dicitonary (fifth edition).

Lin discloses:

The system of claim 1, the self-testing RAM interface is constructed with higher performance memory devices than the memory array (column 4 lines 14-20)

Lin does not disclose:

including Gallium Arsenide based devices

Microsoft Computer Dicitonary defines gallium arsenide as a type of material used to manufacture chips in place of silicon. It provides a faster, more reliable functionality. Lin's system is designed to reduce manufacturing costs and time (column 2 lines 17-23). Using gallium arsenide chips would further prevent reliability issues and enable the memory to perform more quickly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate gallium arsenide into the chips of the memory testing system of Lin, improving reliability and speed.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (United States Patent No. 6,141,768) in view of Wyatt (United States Patent 6,968,479)

As per claim 12, Lin discloses:

The system of claim 1, the self-testing RAM interface comprises large geometry devices (column 4 lines 9-23)

Lin does not disclose:

[the self-testing RAM interface comprises] ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory array.

and ECC

Wyatt discloses an error memory verification system (column 4 lines 9-23) with ECC (column 6 lines 11-18). Wyatt discloses that ECC is a commonly used error correction method helpful in a wide variety of memory devices (column 2 lines 8-31). Lin discloses that any error correction method may be used (Column 4 lines 45-49). Using ECC would enable the Lin's system to detect and isolate the errors in the memory effectively, without storing an entire mirrored copy. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC code into the memory testing system of Lin, improving reliability and speed.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (US Patent No. 6,505,305) in view of Microsoft Computer Dicitonary (fifth edition).

Olarig discloses:

The system of claim 14, the self-testing RAM interface is constructed with higher performance memory devices than the memory array (column 5 lines 38-45)

Olarig does not disclose:

. . . including Gallium Arsenide based devices

Microsoft Computer Dicitonary defines gallium arsenide as a type of material used to manufacture chips in place of silicon. It provides a faster, more reliable functionality. Olarig's invention is designed to save time, reduce failures (column 2 lines 33-40), and accommodate modern high speed computing systems (column 1 lines 15-24). Using gallium arsenide chips would further prevent reliability issues and enable the memory to perform more quickly. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of invention to incorporate gallium arsenide into the chips of the failover system of Olarig, improving reliability and speed.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (US Patent No. 6,505,305) in view of Callaway (6,879,530).

As per claim 18, Olarig fails to disclose:

The system of claim 14, the self-testing R.AM interface acts as a virtual memory manager and maps received data to multiple copies of the data in different memory banks to enable correct data retrieval.

Callaway discloses a multiple redundant system in which identical data is stored in three memory devices. A majority voting system is used to decide which data is faulty (column 10 lines 30-51). Callaway discloses that this enables his invention to detect failed memory blocks and remap the correct blocks to other memory areas (Callaway column 2 lines 44-48). Olarig discloses that the memory is continually monitored for faults (column 10 lines 59-65) and that they will need to be remapped to another location later (column 1 lines 9-13). Using Callaway's dynamic memory repair system would increase the reliability of the data since there are three available sources, and enable the system to write the correct memory to another location if it has already been lost, further increasing reliability. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory repairing

system of Callaway into the chips of the failover system of Olarig, to detect errors and improve reliability.

As per claim 19, Olarig discloses:

The system of claim 18, error correction codes (ECCs) and voting mechanisms determine the most probable data value to return from amongst the multiple copies.

Callaway discloses a multiple redundant system in which identical data is stored in three memory devices. A majority voting system is used to decide which data is faulty (column 10 lines 30-51). Callaway discloses that this enables his invention to detect failed memory blocks and remap the correct blocks to other memory areas (Callaway column 2 lines 44-48). Olarig discloses that the memory is continually monitored for faults (column 10 lines 59-65) and that they will need to be remapped to another location later (column 1 lines 9-13). Using Callaway's dynamic memory repair system would increase the reliability of the data since there are three available sources, and enable the system to write the correct memory to another location if it has already been lost, further increasing reliability. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory repairing system of Callaway into the failover system of Olarig, to detect errors and improve reliability.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Callaway (6,879,530) in view of Microsoft Computer Dicitonary (fifth edition).

Callaway discloses:

The device of claim 20, voting mechanisms determine the most probable data value to return from amongst the plurality of stored copies (column 10 lines 30-51).

Callaway does not disclose:

error correction codes (ECCs) determine the most probable data value

Microsoft Computer Dicitonary defines Error correction coding as a method which detects errors in digital data by encoding it in such a way that it can be examined and errors can be detected and sometimes located. Callaway's system is also designed to detect and correct errors in a memory system (column 1 lines 6-11). Using ECC in the redundant system of system of Chen would enable the system to detect and correct errors on one of the multiple sets of data, or act as an additional failure indication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC coding into the failover system of Olarig, as an added means of redundancy and reliability.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes (US Patent 5,781,721) in view of Microsoft Computer Dicitonary (fifth edition).

As per claim 24, Hayes does not disclose:

The method of claim 22, the central processing unit is notified by generating an interrupt.

Microsoft Computer Dictionary defines an interrupt is a command which is sent to a processor, bringing its attention to a situation. The processor stops its other operations to deal with the cause of the interrupt. Hayes discloses that his system may include steps to repair a memory in a processor (column 5 lines 25-30). Using an interrupt would be a natural first step since it would stop the processor from attempting to complete other operations, and would not attempt to operate while its memory is still in a faulty state. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate interrupts into the testing system of Hayes, as a means for processor repair.

Claims 30-33, 36, 37, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (US Patent No. 6,505,305) in view of Hayes (US Patent 5,781,721).

As per claim 30, Olarig discloses:

A method for detecting hard errors comprising:

writing a test pattern to a plurality of memory cells in a memory device (column 10 lines 55-65);

reading the value of each memory cell containing a portion of the test pattern (column 10 lines 55-65);

recording the number times the value written did not correspond to the value read for each cell, wherein writing a test pattern, reading the value, comparing the

value, and recording the number of times the value written did not correspond to the value read are performed by a self-testing RAM interface (column 10 line 65- column 11 line 20).

Olarig does not disclose:

comparing the value read with the value written to each cell;

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

As per claim 31, Olarig discloses:

The method of claim 30, further comprising:

determining whether any cell or cells have produced erroneous results more than a threshold number of times (column 11 lines 12-27);

determining whether any extra memory cells are available (column 11 lines 50-60); and

mapping any cells that have produced erroneous results more than a threshold number of times to available extra memory cells (column 11 lines 50-60).

As per claim 32, Olarig discloses:

The method of claim 31, further comprising notifying an exception handler if there are no available extra cells (column 11 lines 61-65).

As per claim 33, Olarig discloses:

The method of claim 30, wherein data regarding the number of times a cell value did not correspond to the value read is stored in a memory component located within the self-testing RAM interface (column 11 lines 10-25).

As per claim 36, Olarig fails to disclose:

The method of claim 35 wherein the self-testing RAM interface corrects incorrect data by retrieving a copy of the data from another data source.

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4

line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

As per claim 37, Olarig discloses:

The method of claim 36, wherein the data source is a magnetic disk drive (column 5 lines 43-45).

As per claim 38, Olarig discloses:

The method of claim 36, wherein the data source is cache memory .

Olarig does not disclose any major restraints on the memory array 304 being examined in his system. It is only disclosed that the memory should be stored in blocks of 16, 32, etc. bytes, and have access to a memory bus (column 7 lines 37-42). A cache memory is a frequently used memory device which can access data quickly, and would be perfectly capable of meeting Olarig's restraints. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to incorporate cache into the memory testing system of Olarig, as a capable memory medium for testing.

As per claim 39, Olarig discloses:

The method of claim 36, wherein the data source is one or more standard RAM devices (column 13 lines 55-59).

As per claim 40, Olarig discloses:

The method of claim 39, wherein the RAM devices contain internal flaws such that the device is not fit for ordinary use (column 1 lines 8-12: the purpose of the system is to determine if there are flaws).

As per claim 41, Olarig discloses:

The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by retrieving a copy of the data from another storage device and comparing the retrieved data and the copy.

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as

disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER

MTL

***